Claims

1. An output buffer configured for use within SDRAM applications, said output buffer comprising:

an output element configured for providing an output for said output buffer; and

a predriver circuit configured to control said output element and comprising a limiter circuit configured for limiting a maximum voltage provided from said predriver circuit to said output element.

2. The output buffer according to claim 1, wherein said predriver circuit further comprises at least one predriver pull-up transistor configured between an external supply voltage and said limiter circuit.

3. The output buffer according to claim 2, wherein said predriver circuit further comprises a p-channel pull-up transistor device and an n-channel pull-down transistor device, each of said p-channel pull-up transistor device and said n-channel pull-down transistor device having control terminals configured to receive a control signal, and wherein said limiter circuit is coupled in series between an output terminal of said p-channel pull-up transistor device and said output element.

4. The output buffer according to claim 2, wherein said limiter circuit comprises an n-channel transistor device coupled between said predriver pull-up transistor and said output element.

5. The output buffer according to claim 2, wherein said limiter circuit comprises at least one diode-connected, n-channel transistor device having a terminal connected between said predriver pull-up transistor and said output element.

6. The output buffer according to claim 2, wherein said limiter circuit comprises at least one diode-connected, p-channel transistor device having an output terminal connected between an output terminal of said predriver pull-up transistor and said output element.

7. The output buffer according to claim 2, wherein said limiter circuit comprises at least one diode device connected between an output terminal of said predriver pull-up transistor and said output element.

8. The output buffer according to claim 1, wherein said limiter circuit comprises an n-channel transistor device coupled between an external supply voltage and an input terminal of said predriver pull-up transistor.

9. The output buffer according to claim 1, wherein said limiter circuit is coupled to an internally generated regulated voltage, and said maximum voltage comprises the difference between said internally generated regulated voltage and a threshold voltage of said limiter circuit.

10. The output buffer according to claim 2, wherein said predriver pull-up transistor is coupled to an external supply voltage, and wherein a full amount of said external supply voltage is provided to said gate of said output element so long as said full amount of said external supply voltage is less than said maximum voltage.

11. A predriver circuit for providing a gate voltage to an output pull-down device of an output buffer, said predriver circuit comprising:

at least one predriver pull-up transistor configured to receive a control signal; and

a limiter device coupled between said at least one predriver pull-up transistor and a gate of the output pull-down device, said limiter device being configured to limit a maximum voltage for the output pull-down device.

12. The predriver circuit according to claim 11, wherein said at least one predriver pull-up transistor comprises a p-channel transistor device having a gate configured to receive said control signal.

13. The predriver circuit according to claim 12, wherein said limiter device comprises an n-channel transistor device coupled in series between said predriver pull-up transistor and the gate of said output pull-down device.

14. The predriver circuit according to claim 12, wherein said limiter device comprises a plurality of n-channel transistor devices connected in series, each of said plurality of n-channel transistor devices comprising a diode-configuration, and one of said plurality of n-channel transistor devices having a gate terminal connected between said predriver pull-up transistor and the gate of said output pull-down device.

15. The predriver circuit according to claim 12, wherein said limiter device comprises a plurality of p-channel transistor devices connected in series, each of said plurality of p-channel transistor devices comprising a diode-configuration, and one of said plurality of p-channel transistor devices having a gate terminal connected between said predriver pull-up transistor and the gate of said output pull-down device.

16. The predriver circuit according to claim 12, wherein said limiter device comprises a plurality of diode devices connected in series, with one of said plurality of diode devices having an anode terminal connected between said predriver pull-up transistor and the gate of said output pull-down device.

17. The predriver circuit according to claim 12, wherein said limiter device and said predriver pull-up transistor can be configured to limit slewing of the output buffer based on respective width/length ratios.

18. A method for limiting a maximum gate voltage of an output element in an output buffer, said method comprising the steps of:

receiving a control signal at a control terminal of a predriver pull-up device of a predriver circuit;

providing said maximum gate voltage from said predriver pull-up device to a limiter circuit of said predriver circuit, said limiter device configured between said predriver pull-up device and said output element; and

limiting said maximum gate voltage provided through said limiter circuit to said output element.

19. The method according to claim 18, wherein said step of limiting said maximum gate voltage comprises limiting said maximum gate voltage to an amount not greater than an internally regulated voltage less a threshold voltage of said limiter circuit.

20. The method according to claim 19, wherein said method further comprises the step of reducing a maximum current in an I-V characteristic of said output element.

21. The method according to claim 19, wherein said step of limiting said maximum gate voltage comprises limiting said maximum gate voltage through clamping of said maximum gate voltage based on a diode configuration of said limiter circuit.

22. The method according to claim 21, wherein said step of limiting said maximum gate voltage comprises limiting said maximum gate voltage through clamping of said maximum gate voltage through at least one of a plurality of diode-connected p-channel transistors and a plurality of diode-connected n-channel transistors.

23. An SDRAM output buffer comprising:

a predriver circuit comprising a predriver pull-up transistor coupled to a limiter circuit, said limiter circuit being configured for limiting a maximum voltage provided from said predriver circuit; and

an output pull-down transistor device configured for providing an output for said SDRAM output buffer, said output pull-down transistor device having a control terminal coupled to said limiter circuit.

24. The SDRAM output buffer according to claim 23, wherein said limiter circuit comprises a plurality of diode configured devices, with at least one of said plurality of diode configured devices connected between said predriver pull-up transistor and said control terminal of said output pull-down transistor device.

25. The SDRAM output buffer according to claim 23, wherein said predriver circuit further comprises a p-channel pull-up transistor device and a n-channel pull-down transistor device, each of said pull-up transistor device and said pull-down transistor device having control terminals configured to receive a control signal, and wherein said limiter device is coupled in series between said pull-up transistor device and said control terminal of said output pull-down transistor device.

26. A memory system having an output buffer configured for providing an operating voltage to a memory device, said output buffer comprising:

an output element configured for providing an output for said output buffer; and

a predriver circuit configured to control said output element and comprising a limiter circuit configured for limiting a maximum voltage provided from said predriver circuit to said output element.

27. The memory system according to claim 26, wherein said predriver circuit further comprises at least one predriver pull-up transistor configured between an external supply voltage and said limiter circuit.

28. The memory system according to claim 27, wherein said predriver circuit further comprises a p-channel pull-up transistor device and an n-channel pull-down transistor device, each of said p-channel pull-up transistor device and said n-channel pull-down transistor device having control terminals configured to receive a control signal, and wherein said limiter circuit is coupled between an output terminal of said p-channel pull-up transistor device and said output element.

29. The memory system according to claim 27, wherein said limiter circuit comprises an n-channel transistor device coupled between said predriver pull-up transistor and said output element.

30. The memory system according to claim 27, wherein said limiter circuit comprises at least one diode-connected, n-channel transistor device having a terminal connected between said predriver pull-up transistor and said output element.

31. The memory system according to claim 27, wherein said limiter circuit comprises at least one diode-connected, p-channel transistor device having an output terminal connected between an output terminal of said predriver pull-up transistor and said output element.

32. The memory system according to claim 27, wherein said limiter circuit comprises at least one diode device connected between an output terminal of said predriver pull-up transistor and said output element.

33. The memory system according to claim 26, wherein said limiter circuit comprises an n-channel transistor device coupled between an external supply voltage and an input terminal of said predriver pull-up transistor.

34. The memory system according to claim 26, wherein said limiter circuit is coupled to an internally generated regulated voltage, and said maximum voltage comprises the difference between said internally generated regulated voltage and a threshold voltage of said limiter circuit.

35. The memory system according to claim 27, wherein said predriver pull-up transistor is coupled to an external supply voltage, and wherein a full amount of said external supply voltage is provided to said gate of said output element so long as said full amount of said external supply voltage is less than said maximum voltage.

36. An electronic system comprising a processor, a supply and a memory system, said memory system having an output buffer comprising:

a predriver circuit comprising a predriver pull-up device coupled to a limiter circuit, said limiter circuit being configured for limiting a maximum voltage provided from said predriver circuit; and

an output element configured for providing an output for said output buffer, said output element having a control terminal coupled to said limiter circuit.

37. The electronic system according to claim 36, wherein said limiter device comprises a plurality of diode configured devices, with at least one of said plurality of diode configured devices connected between said predriver pull-up device and said control terminal of said output element.

38. The electronic system according to claim 36, wherein said predriver circuit further comprises a p-channel pull-up transistor device and a n-channel pull-

down transistor device, each of said pull-up transistor device and said pull-down transistor device having control terminals configured to receive a control signal, and wherein said limiter device is coupled between said pull-up transistor device and said control terminal of said output element.